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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 81862.P116 Total Pages 5

First Named Inventor or Application Identifier Onchuen D. Lau

Express Mail Label No. EL143554367US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. x Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. x Specification (Total Pages 17)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. x Drawings(s) (35 USC 113) (Total Sheets 4)

4. x Oath or Declaration (Total Pages 5)

a. x Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. _____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__x__ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. __x__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
_____ b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. __x__ Other: Copy of the Postcard w/Express Mail Stamp

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
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Attorney's Docket No.: 081862.P116 Patent

United States Patent Application

For

SCHEME FOR MAINTAINING SYNCHRONIZATION IN AN INHERENTLY ASYNCHRONOUS SYSTEM

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SCHEME FOR MAINTAINING SYNCHRONIZATION IN AN INHERENTLY ASYNCHRONOUS SYSTEM

FIELD OF THE INVENTION

The present invention relates to a scheme for synchronizing operations among distributed components of a digital system, for example an ATM switch, that are inherently asynchronous.

BACKGROUND

Many digital systems, for example ATM or other communication switches, are made up of a number of components that are physically located on different printed circuit (PC) boards. The boards are housed in a chassis and are interconnected to one another through signal paths that make up a backplane within the chassis. When the distances between the PC boards is small and/or the system is operated at low speed, it is relatively straight forward to maintain synchronization between the various components. For example, at low operating speeds, the skew among various components caused by relative differences in signal path lengths between the PC boards may cause operational problems. Then, as the PC boards become larger and/or as operating speeds are increased, maintaining synchronization between the components becomes even more difficult and one cannot simply rely on trying to maintain equal signal path lengths. Moreover, if propagation delays along the signal path traces are long (e.g., so long as to exceed one clock period), additional operating problems may be encountered.

What is needed therefore, is a means for ensuring synchronization within an inherently asynchronous system such as a digital switch or other device that is made up of various components physically located on PC boards and the like.

SUMMARY OF THE INVENTION

In one embodiment, a synchronization state for a local clock generating circuit of a first of a number of components of a distributed system is maintained according to a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to the components within the distributed system. The local clock generating circuit may enter the synchronization state only after observing a predetermined number of occurrences of successive local clock cycles between instances of the global synchronization signal. Generally, the local clock generating circuit provides local control signals for the first of the components at time instants corresponding to the number of local clock cycles.

In the present scheme, the local clock generating circuit continues to provide local control signals for the first of the components at time instants corresponding to the number of local clock cycles even after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more or less than the number of local clock cycles. However, the local clock generating circuit enters an alarm state when the global synchronization signal is observed at time instants corresponding to more than one local clock cycle more or less than the number of local clock cycles.

The local clock generating circuit may enter a missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles. From this state, the local clock generating circuit returns to the synchronization state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles. However, the local clock generating circuit enters the alarm state from the missing clock state after an instance of the global

synchronization signal is observed at a time instant corresponding to two or more local clock cycles less than the number of local clock cycles.

The local clock generating circuit may also enter an extra clock state from the synchronization state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles. From this state, the local clock generating circuit returns to the synchronization state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles. However, the local clock generating circuit enters the alarm state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to two or more local clock cycles more than the number of local clock cycles.

Other features and advantages of the present scheme will be apparent from the following discussion.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements and in which:

Figure 1 illustrates an example of a communication switch within which the synchronization methodologies described herein may be practiced;

Figure 2 illustrates an example of the physical layout the communication switch shown in Figure 1;

Figure 3 is a state diagram for a local clock generating circuit configured in accordance with the present synchronization scheme; and

Figure 4 illustrates an example of timing skews which may be compensated for using the present synchronizing scheme.

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DETAILED DESCRIPTION

A scheme for maintaining synchronization among various components of an inherently asynchronous system such as a digital switch or other device that is made up of various components physically located on PC boards and the like is disclosed herein. Although discussed with reference to certain illustrated embodiments, upon review of this specification, those of ordinary skill in the art will recognize that the present scheme may find application in a variety of systems. Therefore, in the following description the illustrated embodiments should be regarded as exemplary only and should not be deemed to be limiting in scope.

An example of one system within which the present synchronization scheme may be implemented is shown in Figure 1. In the diagram, various components of a digital switch (e.g., an ATM or other communication switch) 10 are shown. In general, the switch 10 includes a number of interface or line cards 12, each or some of which may include functional circuitry blocks 14a - 14c.

While Figure 1 illustrates the logical layout of switch 10, Figure 2 illustrates its physical layout. As shown, switch 10 may include several line cards 12, each of which may be substantially similar and each of which may include both inbound and outbound functional circuitry blocks. One or more switch cards 18 may also be included within switch 10, each of which may be substantially similar to one another and each of which may include switching functional circuitry. Although not shown in this illustration, it is generally the case that any line card 12 may switch packets to any other line card 12 through any of the switch cards 18 using communication paths that interconnect these cards.

Also included in switch 10 is a control or clock signal generating card 20. Often, the clock signal generating card 20 will produce global clock signals and other control signals

that are routed to the line cards 12 and the switch cards 18 across a backplane 22. Backplane 22 is thus made up of a number of communication signal paths and may also include the communication signal paths that transport the packets between the line cards 12 through the switch cards 18.

Where switch 10 does not operate at high speeds and/or where the distances across backplane 22 and/or the various cards of switch 10 are small, maintaining synchronization among the various operational components of the cards is relatively straightforward. As indicated above, such synchronization can usually be ensured by ensuring that the signal path lengths across backplane 22 are kept relatively uniform. However, as the physical distances across the backplane 22 increase (e.g., due to larger physical cards) and/or as the operation speed of switch 10 increases, ensuring synchronization becomes nontrivial. Simply relying on global signals produced by a control or clock signal generating card 20 is not sufficient, because those signals may not be received by each of line cards 12 and/or switch cards 18 at the same time instant. Any timing skews between the various cards can lead to operational problems for switch 10.

Rather than simply relying on such global clock signals, the present synchronization scheme employs both locally generated (i.e., on-card) clock signals as well as global synchronization signals. In brief, each card (e.g., line cards 12 and switch cards 18) maintains a local clock signal (e.g., as produced using a local clock (LC) circuit 24), which is used to control operations on that card. Further, a global synchronization signal that is generated by circuitry on the clock signal generating card 20 once every "n" clocks (i.e., once every "n" clock cycles of the local card clocks) is provided to the other cards (e.g., line cards 12 and switch cards 18) of switch 10 via backplane 22. By keeping track of where (i.e., at what time instant) the global synchronization signal is observed relative to the

number of local clock cycles that have expired since the last occurrence thereof, each card of switch 12 can maintain synchronization to the other cards.

In one embodiment, each card (e.g., line cards 12 and switch cards 18) includes an LC circuit 24 that includes a local counter. The LC circuits 24 are used to generate local clock signals for their respective cards. Local circuitry for each card utilizes the local clock signals produced by the LC circuits 24 associated therewith. The counters of the various LC circuits 24 may be reset by a global synchronization (synch) signal transmitted from the clock signal generating card 24 across the backplane 22.

As shown in Figure 3, each LC circuit 24 is also operated under the control of a state machine 30. At the outset, the LC circuits 24 are in an initialization state 32. In this state, the LC circuits 24 count the number of successive occurrences of the global synchronization signal that are received at intervals of n local clock cycles. If "m" (e.g., m = 8) consecutive occurrences of the global synchronization signal are observed at intervals of n (e.g., n = 62) local clock cycles, then the LC circuit 24 enters a "locked" state 34. In general, n may correspond to the number of local clock signals between locally generated control signals for a card. The locked state 34 corresponds to a situation in which the LC circuit 24 is operating in synchronization with the LC circuits 24 of other cards in switch 10. As shown, for each occurrence of the global synchronization signal that is observed after n local clock cycles, the LC circuit 24 remains in the locked state 34.

Because of differing signal path lengths, temperature variations, process variations, and other operating conditions, it can be expected that, over time, an LC circuit 24 associated with a card of switch 10 may observe a global synchronization signal "early" or "late" with respect to the anticipated arrival at n clock cycles. For example, the global synchronization signal may be observed at n-1 clocks (early) or n+1 clocks (late).

Where the global synchronization signal is observed at n-1 clocks, the LC circuit 24 enters the "short" state 36. In this state, local control signals for the card are still generated once every n clock cycles. However, there exists a mismatch between the global synchronization signal and the local control signal. The LC circuit 24 will remain in the short state so long as successive occurrences of the global synchronization signal are observed at n clock cycles. If the "missing" clock cycle is observed, that is if the global synchronization signal is observed at n+1 clocks, the LC circuit returns to the locked state 34. If, however, the global synchronization signal is again observed at n-1 clocks, this is an indication that the LC circuit 24 has lost synchronization and the LC circuit 24 enters an alarm state 38.

From the locked state 34, if the global synchronization signal is observed at n+1 clocks, the LC circuit 24 enters a "long" state 40. In this state, local control signals for the card are still generated once every n clock cycles. However, there exists a mismatch between the global synchronization signal and the local control signal. The LC circuit 24 will remain in the long state so long as successive occurrences of the global synchronization signal are observed at n clock cycles. If the "extra" clock cycle is consumed, that is if the global synchronization signal is observed at n-1 clocks, the LC circuit returns to the locked state 34. If, however, the global synchronization signal is again observed at n+1 clocks, this is an indication that the LC circuit 24 has lost synchronization and the LC circuit 24 enters the alarm state 38.

Where more than a single clock cycle difference exists between the global synchronization signal and n occurrences of the local clock signal, this is an indication that the LC circuit has lost synchronization and the LC circuit 24 will enter alarm state 38. In this state, error flags may be set that can indicate a fault condition to other components of the

card hosting the LC circuit 24. Local control signals may still be generated every n clocks, however, it is preferable that the error flags cause a local control processor to reset the LC circuit 24 to the initialization state 32, in an attempt to reacquire synchronization.

For sake of clarity, Figure 4 shows an example of where a global synchronization signal (S) is observed at one card (C2) at a time corresponding to n local clock cycles, but is not observed at another card (C1) until n+1 local clock cycles. Assume cards C1 and C2 each include a local clock circuit that produces a clock signal substantially similar to that shown by signal clk. If at a time t = 0, with respect to the signal clk, the global synchronization signal S is produced by a clock generating card, then that signal S will eventually propagate (e.g., across the backplane) to cards C1 and C2. However, because of the varying lengths of the communication signal paths between the cards, the signal S may be observed at different times at C1 and C2. For example, in the figure the signal S is observed (e.g., by latching the logic high value of signal S) at card C2 at a time corresponding to clock cycle n. That is, the signal S arrives a sufficient time (t_{setup} or more) in advance of clock cycle n so that its logic high state is latched or otherwise captured on the rising edge of clk. However, the same signal S is not observed at card C1 until clock cycle n+1, because signal S does not arrive at C1 until a time t_{hold} or more after the rising edge of clk at cycle n. Similar timing skews may cause signal S to be observed at a time corresponding to a clock cycle n-1.

The above synchronization scheme allows the various timing skews to be compensated for and allows synchronization to be maintained in systems such as switch 10 that tend to be inherently asynchronous because of the use of independent local clock signal generators (e.g., LC circuits 24).

Thus a scheme for maintaining synchronization among various components of an inherently asynchronous system such as a digital switch or other device that is made up of various components physically located on PC boards and the like has been described. Although the foregoing description and accompanying figures discuss and illustrate specific embodiments, it should be appreciated that the present invention is to be measured only in terms of the claims that follow.

CLAIMS

What is claimed is:

1. A method comprising maintaining a synchronization state for a local clock generating circuit of a first of a number of components of a distributed system according to a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to the components within the distributed system.

2. The method of claim 1 wherein the local clock generating circuit enters the synchronization state only after observing a predetermined number of occurrences of successive local clock cycles between instances of the global synchronization signal.

3. The method of claim 2 wherein the local clock generating circuit provides local control signals for the first of the components at time instants corresponding to the number of local clock cycles.

4. The method of claim 3 wherein the local clock generating circuit continues to provide local control signals for the first of the components at time instants corresponding to the number of local clock cycles even after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more or less than the number of local clock cycles.

5. The method of claim 3 wherein the local clock generating circuit enters an alarm state when the global synchronization signal is observed at time instants corresponding to more than one local clock cycle more or less than the number of local clock cycles.

6. The method of claim 3 wherein the local clock generating circuit enters a missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

7. The method of claim 6 wherein the local clock generating circuit returns to the synchronization state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

8. The method of claim 6 wherein the local clock generating circuit enters an alarm state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one or more local clock cycle less than the number of local clock cycles.

9. The method of claim 3 wherein the local clock generating circuit enters an extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

10. The method of claim 9 wherein the local clock generating circuit returns to the synchronization state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

11. The method of claim 9 wherein the local clock generating circuit enters an alarm state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to two or more local clock cycles more than the number of local clock cycles.

12. A system comprising a number of asynchronous components coupled to one another through one or more communication signal paths, one or more of the components including local clock generating circuits configured to generate local control signals, each of the local clock circuits being synchronized with one another according to a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to the components within the system.

13. The system of claim 12 wherein each of the local clock generating circuits is configured to enter the synchronization state only after observing a predetermined number of occurrences of successive local clock cycles between instances of the global synchronization signal.

14. The system of claim 13 wherein the local clock generating circuits are further configured to continue to provide local control signals for their respective components at time instants corresponding to the number of local clock cycles even after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more or less than the number of local clock cycles.

15. The system of claim 13 wherein the local clock generating circuits are configured to enter an alarm state when the global synchronization signal is observed at time instants corresponding to more than one local clock cycle more or less than the number of local clock cycles.

16. The system of claim 13 wherein the local clock generating circuits are configured to enter a missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

17. The system of claim 16 wherein the local clock generating circuits are configured to return to the synchronization state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

18. The system of claim 16 wherein the local clock generating circuits are configured to enter an alarm state from the missing clock state after an instance of the global synchronization signal is observed at a time instant corresponding to two or more local clock cycles less than the number of local clock cycles.

19. The system of claim 13 wherein the local clock generating circuits are configured to enter an extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more than the number of local clock cycles.

20. The system of claim 19 wherein the local clock generating circuits are configured to return to the synchronization state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle less than the number of local clock cycles.

21. The system of claim 19 wherein the local clock generating circuits are configured to enter an alarm state from the extra clock state after an instance of the global synchronization signal is observed at a time instant corresponding to one or more local clock cycle more than the number of local clock cycles.

22. The system of claim 12 wherein the components comprise line and/or switch cards of a communications switch.

ABSTRACT

A synchronization state for a local clock generating circuit of a first of a number of components of a distributed system is maintained according to a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to the components within the distributed system. The local clock generating circuit may enters the synchronization state only after observing a predetermined number of occurrences of successive local clock cycles between instances of the global synchronization signal. The local clock generating circuit continues to provide local control signals for the first of the components at time instants corresponding to the number of local clock cycles even after an instance of the global synchronization signal is observed at a time instant corresponding to one local clock cycle more or less than the number of local clock cycles. However, the local clock generating circuit enters an alarm state when the global synchronization signal is observed at time instants corresponding to more than one local clock cycle more or less than the number of local clock cycles.

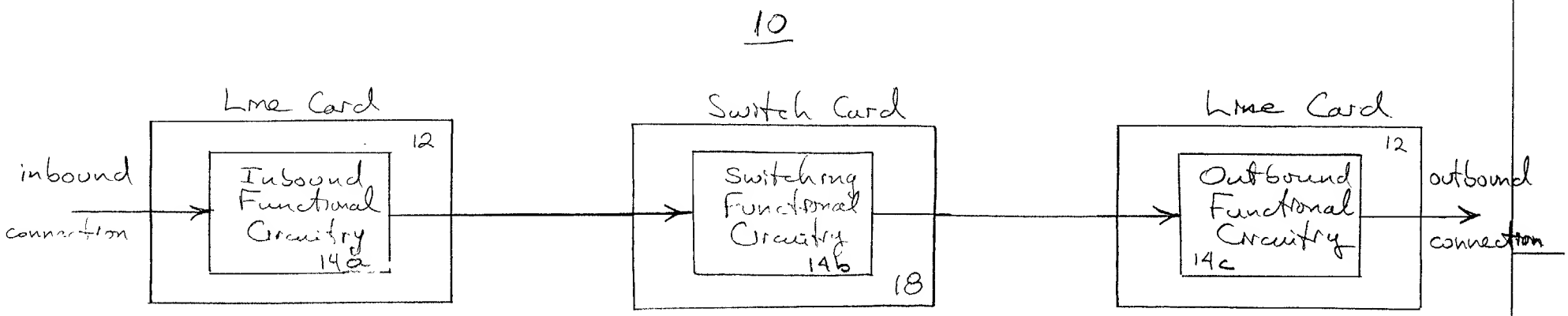

Fig. 1

10

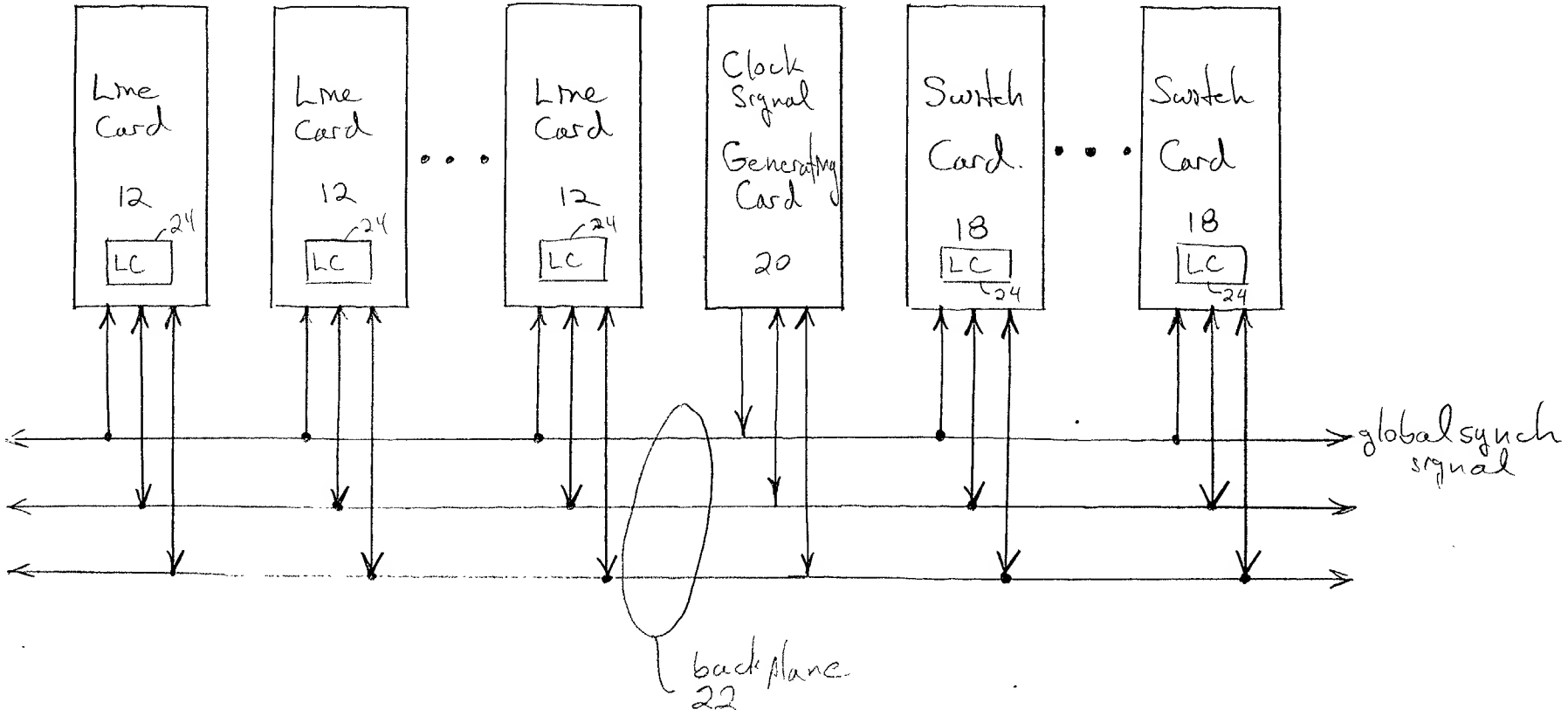

Fig. 2

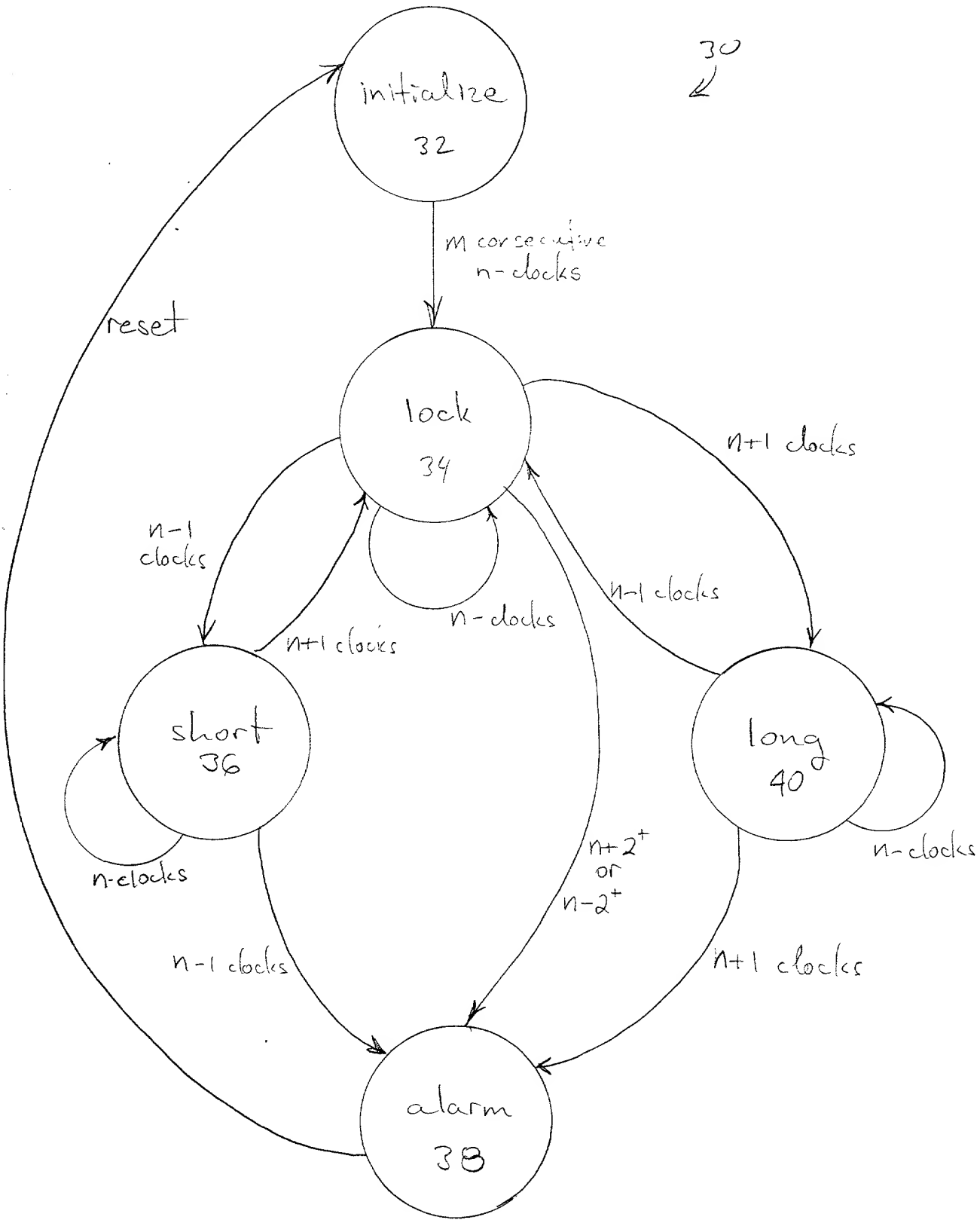

Fig. 3

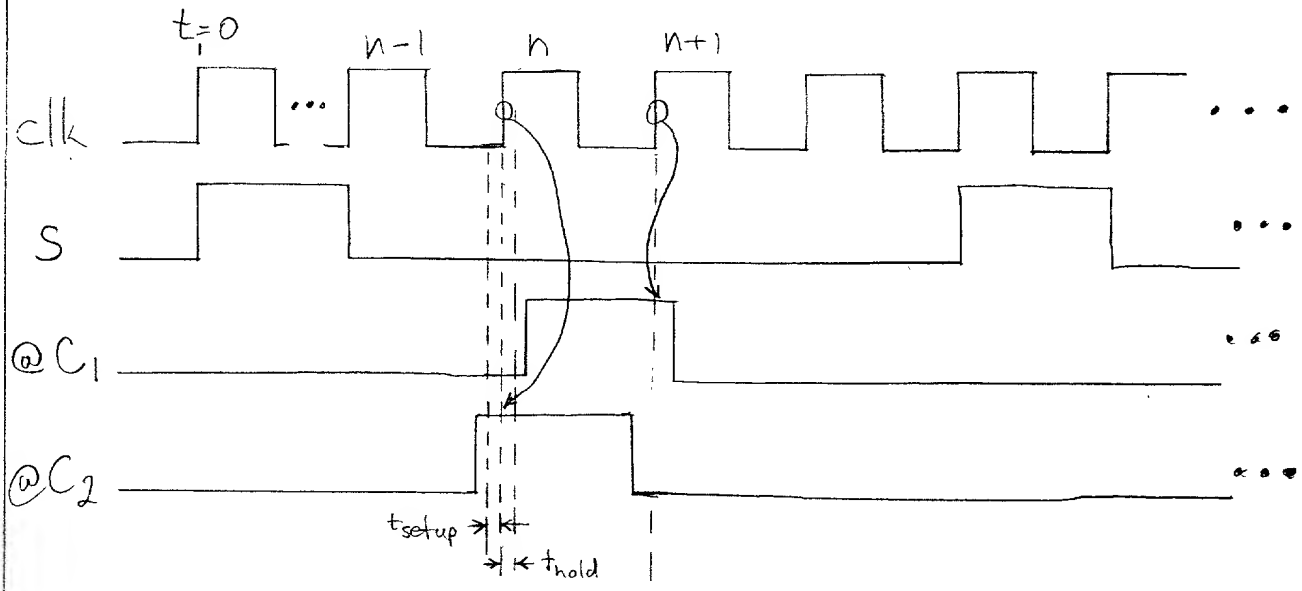

Fig. 4

Attorney's Docket No.: 81862.P116 PATENT

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As a below named inventor, I/We hereby declare that:

My/Our residence(s), post office address(es) and citizenship are as stated below, next to my/our name(s).

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SCHEME FOR MAINTAINING SYNCHRONIZATION IN AN INHERENTLY ASYNCHRONOUS SYSTEM

the specification of which

__X__ is attached hereto.
____ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

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Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

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(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are

punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.